



PROJECT HYDRA – HOW THE BOOST WORKS

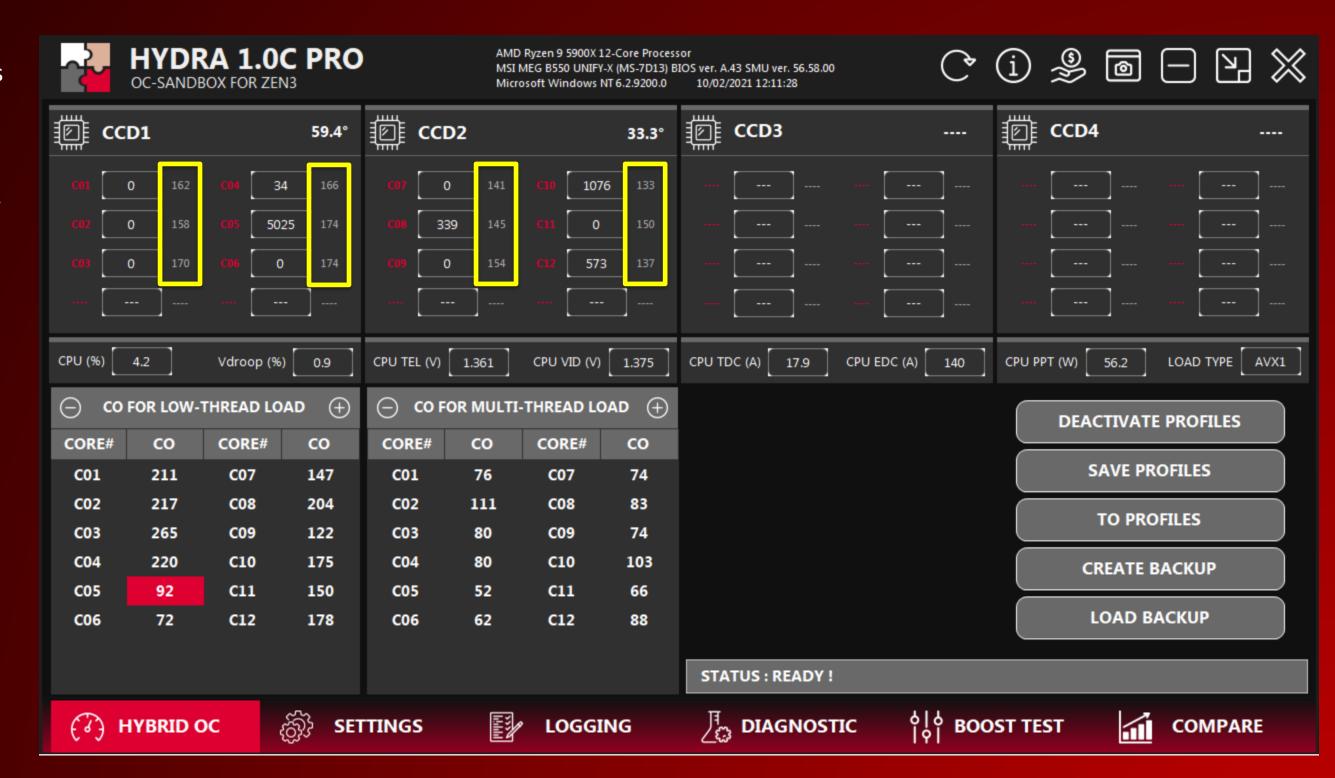
The main task of the Windows thread scheduler is to distribute task execution among the best cores depending on the CPPC rating. The higher the CPPC value, the more likely it is that the task will be run on that core. If the load is multi-threaded - the maximum frequency will depend on the rating of the core with the worst CPPC tag currently in use.

In the case of Ryzen processors, there are always two top cores with the same CPPC tags in the system which creates a number of difficulties.

To achieve maximum performance, HYDRA is able to change the frequency of profiles in real time at very high speed (~100 times per second).

HYBRID OC is the name of the technology which manages the frequency of each CCD individually. This technology has several modes that I want to consider on the example of a single-thread load:

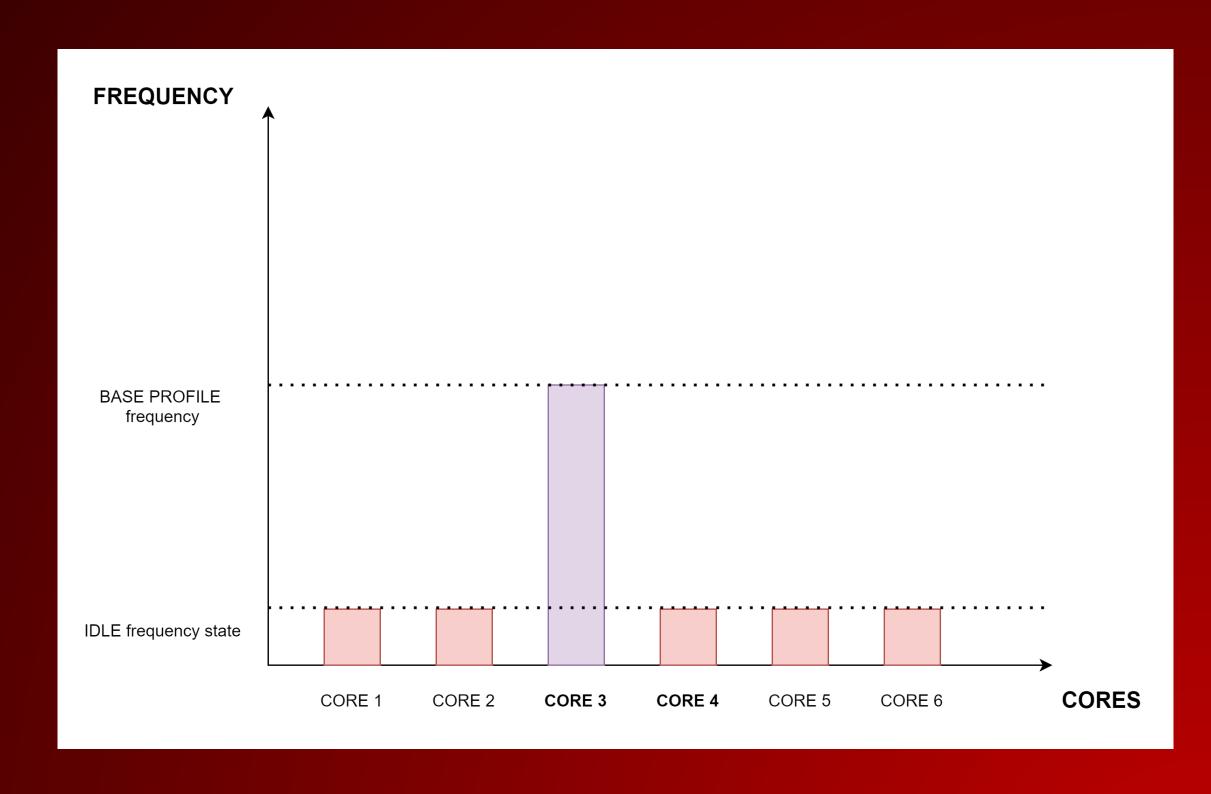
Standard and Frequency lock mode.



In order to engage the right core, HYDRA evaluates the activity of the cores on a number of parameters, in particular the key role played by triggers: CO (core activity) and CAC trigger (EDC throttling). These settings can be controlled by the user (SETTINGS tab).

CYCLE 1

Then the base frequency of the corresponding profile is set for all active cores. All unloaded cores are blocked at a frequency equal to the profile frequency minus 1000 MHz.

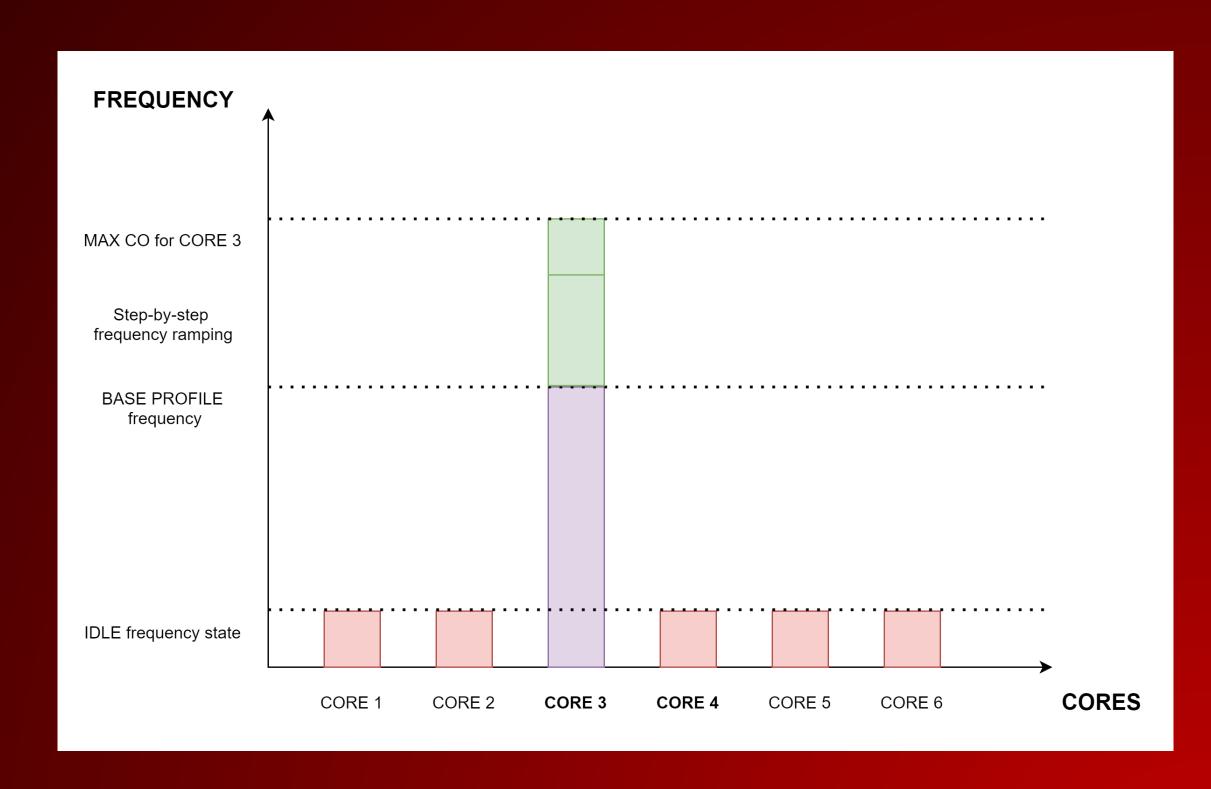


CYCLE 2

After the base frequency has been set, HYDRA evaluates the CO table for the active cores, calculates the safe surplus frequency and sets it. That is, it makes a serious frequency jump.

CYCLE 3 - 4 - 5 (for example)

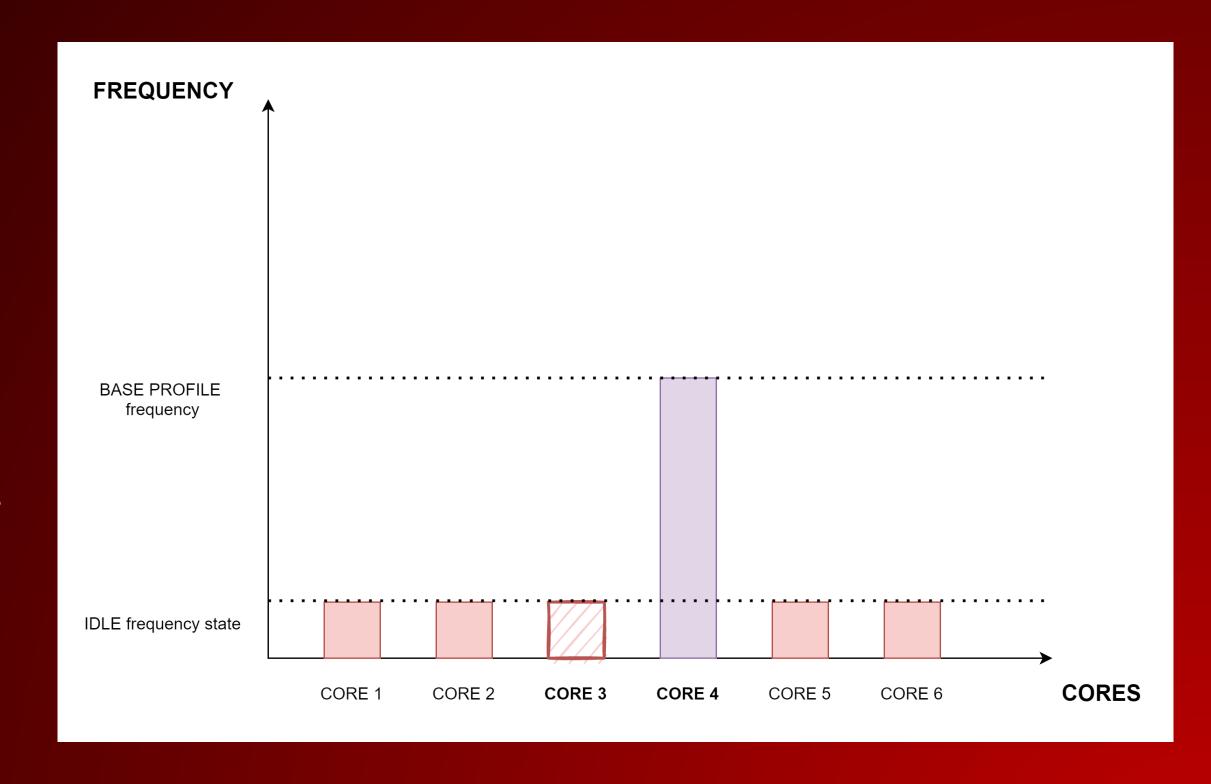
Accurate frequency tuning is performed. But.



CYCLE 6

Because the two top cores have the same CPPC tags, the Windows thread scheduler may think that the current task should be performed on the other core (context-switching). As a consequence HYDRA will be forced not to hold the maximum frequency on the core which was used, but to switch the frequency to the new core and rebuild the frequency.

Again we evaluate which cores are active and set them to the base frequency of the corresponding profile.



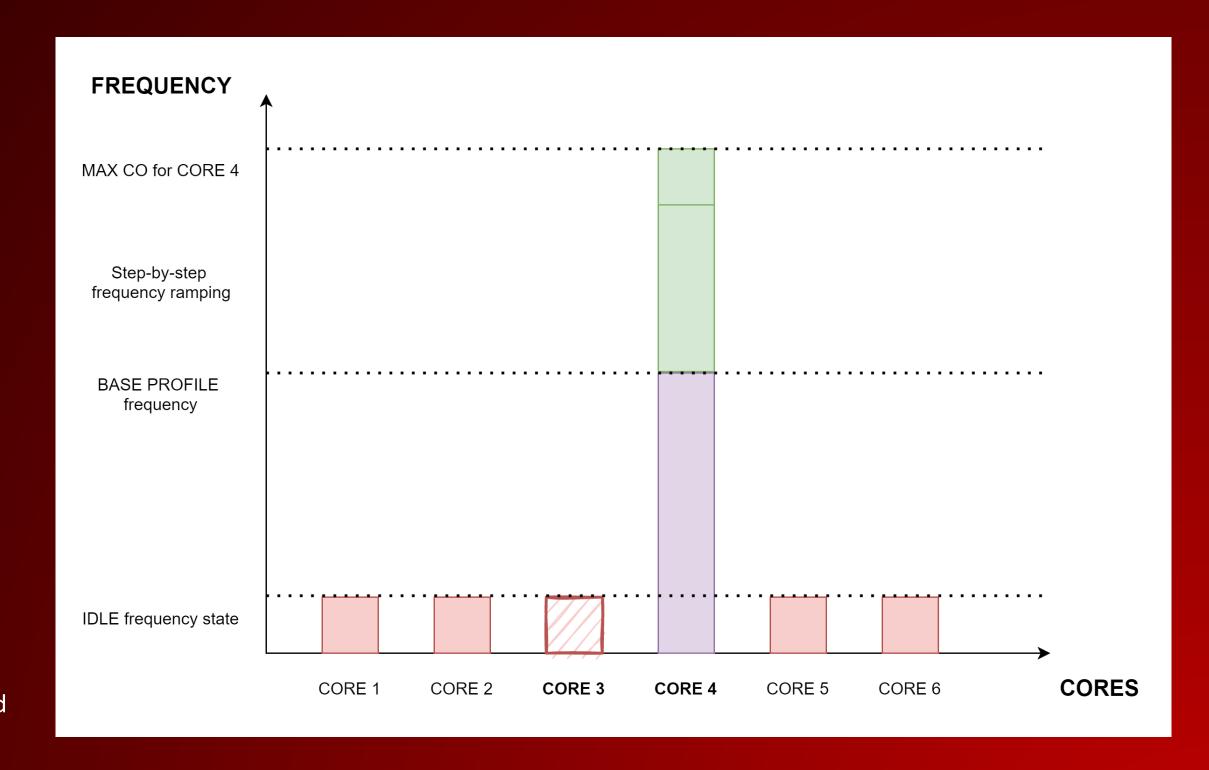
CYCLE 7+

Similarly to CYCLES 2, 3 and 4, the frequency is ramped up (if the list of active cores is still the same).

Besides the thread scheduler problem, there is another problem that seriously affects the performance of user systems: the background activity of all existing processes on the system. First and foremost, these are services like Origin, Steam, and so on. Secondly, these are monitoring and RGB management programs. At the end of the list are programs that ignore CPPC.

Any program on this list can cause context switching, which will cause HYDRA to set the base frequency, and after making sure the load has not changed, start ramping up the frequency.

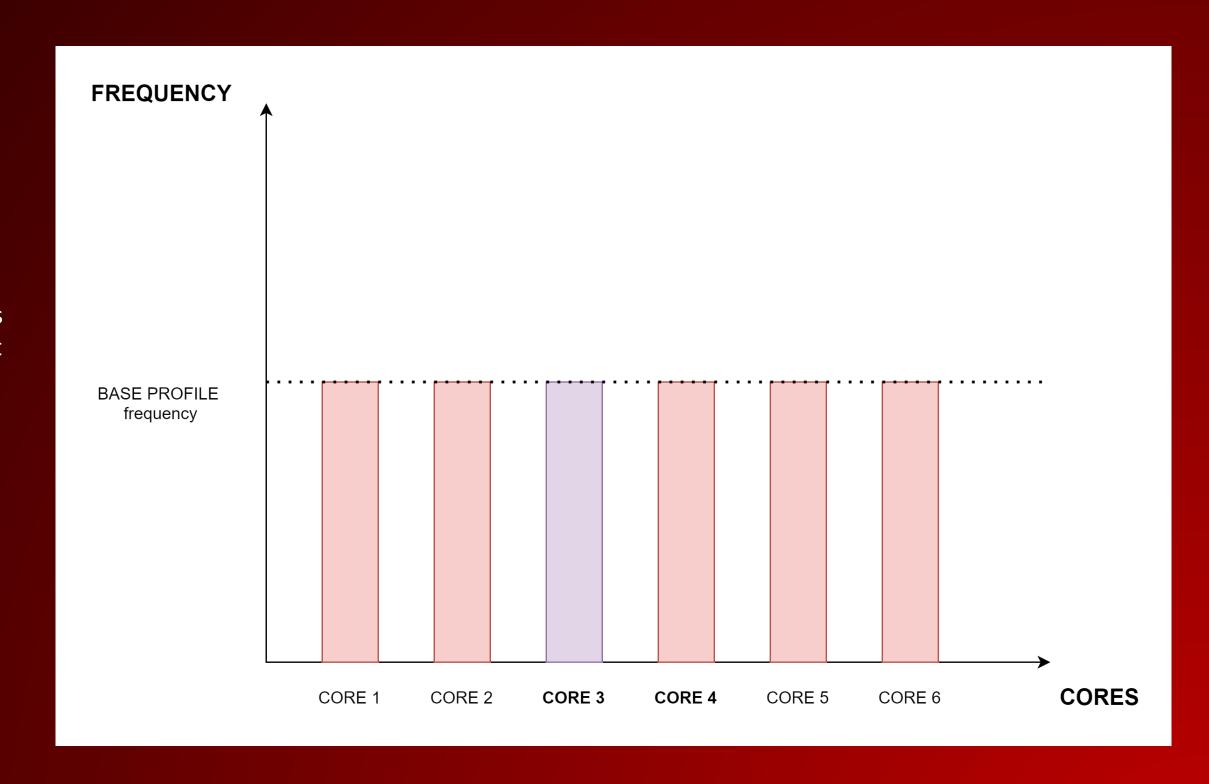
If it happens every few ms, it becomes a disaster. The maximum the user can count on is the base frequency of the profile. In order to reduce spam in profile/frequency switching, a new frequency control mode has been developed - Frequency lock mode.



CYCLE 1

The point of this mode is to predict to prevent useless actions of the thread scheduler and to save the system from constant reassessment of active cores with subsequent frequency ramping.

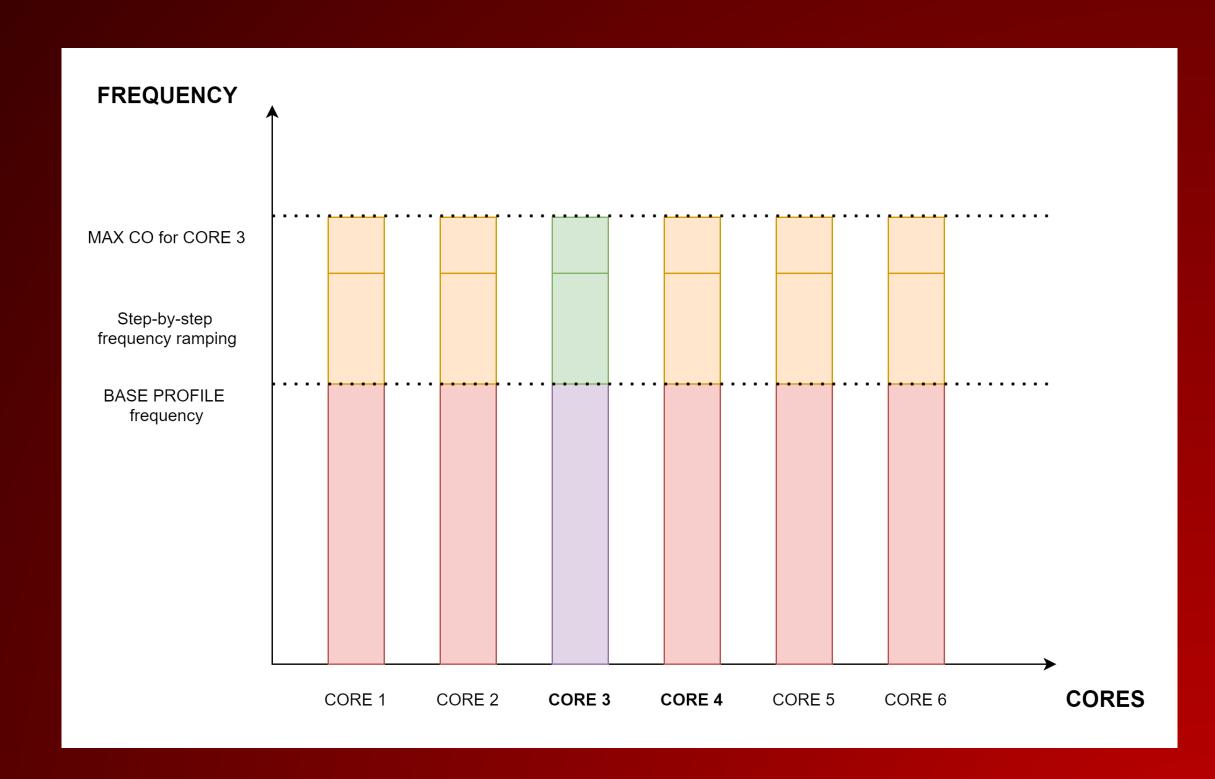
Regardless of the number of active or used cores, the base frequency of the corresponding profile is set for the entire CCD.



CYCLE 2 - 3 - 4 (for example)

After the CO evaluation for each of the cores (each CCD), the frequency is ramped up, and on the next cycle the frequency is fine-tuned.

CCDs that are not loaded remain running at the base profile frequency to avoid overboost during their own inactivity or background system activity.



CYCLE 5+

Switching the context or changing the list of active cores does not cause the frequency to reset to the base value of the corresponding profile.

The same cycle is used to fine-tune the frequency depending on CO values.

This means that the background activity of Windows and a number of other applications no longer affect the maximum frequency under low-thread load.

